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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,165	01/18/2002	Katsuhiko Fukasaku	NE253-US	7604

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EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/050,165

Applicant(s)

FUKASAKU, KATSUHIKO

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 7, 8 and 11-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 7, 8 and 11-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 7, 8, 11, 12, 19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (US 6020229), hereafter Yamane in view of Chien et al. (US 6432768).

Regarding claims 1-3, 7, 8, 11 and 12, Fig.10 of Yamane shows a semiconductor device comprising:

a plurality of transistors on formed on a substrate (201) comprising I/O-purpose MOSFET (col. 8, lines 38-40) with a thicker gate insulator film (30nm) and a thicker gate electrode (200nm) than a core-purpose MOSFET (LV transistor; col.9, line 5) which has a thickness of 10nm for a gate insulator film and 100nm for a gate electrode; and the said gate electrode includes an impurity to suppress depletion when forming a source region and a drain region (col. 5, lines 46-59; col. 6, lines 58-60; col.8, lines 42-44).

Yamane fails to show a device having a Ldd formation with a depth corresponding the thickness of the gate and the gate insulator film. Fig. 1F of Chien shows Ldd regions (132, 116) for gates corresponding to the thickness of the gate and the gate insulator film. It would have been obvious to one of ordinary skill to use the teaching of Chien to the device of Yamane in

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order to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage , migrating of the hot carriers and inhibiting short channel effect.

In detail, Fig. 1F of Chien shows that a thicker gate (112) with a deeper Ldd region(116) and a thinner gate(124) with a shallow Ldd region(134). It would be obvious that a deeper Ldd region is formed with a thicker gate since the Ldd region of Chien is formed using the gate as a mask (col. 2, line 51- col. 3, line 20).

Regarding claim 19, Fig. 1F of Chen shows a device comprising a plurality of sidewalls and a thicker gate having a higher sidewalls.

Regarding claims 22 and 23, Fig.10 of Yamane shows a semiconductor device comprising:

a plurality of transistors on formed on a substrate (201) comprising I/O-purpose MOSFET (col. 8, lines 38-40) with a thicker gate insulator film (30nm) and a thicker gate electrode (200nm) than a core-purpose MOSFET (LV transistor; col.9, line 5) which has a thickness of 10nm for a gate insulator film and 100nm for a gate electrode; and the said gate electrode includes an impurity to suppress depletion when forming a source region and a drain region (col. 5, lines 46-59; col. 6, lines 58-60; col.8, lines 42-44).

Yamane fails to show a device having a Ldd formation with a depth corresponding the thickness of the gate and the gate insulator film. Fig. 1F of Chien shows Ldd regions (132, 116) for gates corresponding to the thickness of the gate and the gate insulator film. It would have been obvious to one of ordinary skill to use the teaching of Chien to the device of Yamane in order to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage , migrating of the hot carriers and inhibiting short channel effect.

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Fig. 1F of Chien shows that a thicker gate(116) with a deeper Ldd region(116) and a thinner gate(124) with a shallow Ldd region(134). It would be obvious that a deeper Ldd region is formed with a thicker gate since the Ldd region of Chien is formed using the gate and the sidewall as a mask (col. 2, line 51- col. 3, line 20). And it would have been obvious to one of ordinary skill to incorporate the teaching of Chien to the device of Yamane to use the gate and the sidewall as a mask to form a Ldd region for self-aligning advantage.

Claims 13-18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane and Chien as applied to claim 1 above, and further in view of Tsao et al. (US 6143594), hereafter Tsao.

Regarding claims 13 and 14, the combined teaching of Yamane and Chien shows substantially the entire claimed structure except the device polarity and the supply voltages. Fig. 1F of Tsao shows a core NMOS and a high voltage NMOS(an I/O purpose NMOS).

The teachings of Yamane and Chien do not show the supply voltage for the core and I/O devices. Tsao shows the operating voltages for core device and the high voltage device. It would have been obvious to one of ordinary skill to use the teaching of Tsao to the device of Yamane and Chien in order to obtain proper operating voltages for electrical function of the device. And it would be obvious to use NMOS for the device of Yamane and Chien since an NMOS is most commonly used for a semiconductor device.

In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an intended supply voltage as recited in pending claim, since it has been

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held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 15, 17 and 20, Fig. 1F of Tsao shows a P-well formation (102) in a core NMOS region and a high voltage NMOS region along with Ldd regions. It is well known in the art that phosphorous and arsenic are the most commonly used material for N-type impurity. Also see a respective portion of Mori et al. (US 6376879) for impurity material.

Note that “implant” is a process designation and would thus not carry patentable weight in his claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 16, 18 and 21, Tsao discloses a density at energy level for HV transistor and LV transistor. In addition it would have been obvious to one of ordinary skill in the art at the time of the invention made to have an intended value for a density for phosphorous and arsenic in a HV and a LV regions as claimed, since it has been that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

Applicant's arguments filed January 10, 2004 have been fully considered but they are not persuasive.

Applicant argues that the devices of Yamane and Chien are not compatible to incorporate the teachings to one another. And the similar argument is made against the device of Tsao.

However, all three of the devices are used for memory applications with essentially the same transistor structure while having a modification in a core element of the transistor structure such as a gate or a source/a drain. It is pointed out that Applicant's speculation/assumption over the particular functionality on the devices does not carry a patentable weight for a device claim.

Applicant further contends that Yamane does not disclose Ldd regions, however, this deficiency is complemented with the Chien's reference. On the contrary to Applicant contention that Chien does not explain why the Ldd regions are provided, Chien explicitly teaches that a Ldd region is formed by implantation through using a gate as a mask. Therefore, it follows that a higher the gate structure is, the deeper the Ldd region is. Additionally, it is known to one of ordinary skill in the art that Ldd regions are provided to have an advantage stated in the Office Action above.

Finally, an allegation regarding hindsight considerations, it is noted that Examiner's conclusion of obviousness is based on a reconstruction through *permissible* hindsight reasoning. For the conclusion of obviousness presented above, Examiner relied only on the knowledge that was available to one of ordinary skill in the art at the time of invention, not including knowledge gleaned only from the Applicant's disclosure.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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